CLAIMS

1. A device for sending/receiving digital data and capable of processing different bit rates from a group of predetermined bit rates, said device including a channel coding/decoding stage including interleaving means (MET) and deinterleaving means (MDET) including a memory (MM) whose minimum size is fixed as a function of the maximum bit rate of said group and having a first memory space (ESM1) assigned to the interleaving means and a second memory space (ESM2) assigned to the deinterleaving means, the size of each of the two memory spaces being parameterable as a function of the bit rate actually processed by the device.

2. A device according to claim 1, characterized in that the channel coding/decoding stage includes Reed-Solomon coding/decoding means (CRS, DCRS) of length N, in that the interleaving means (MET) are adapted to effect convolutional interleaving of I branches with $\underline{i} - 1$ blocks of M bytes and the deinterleaving means are adapted to implement convolutional deinterleaving with I' branches of $i' - 1$ blocks of M' bytes, I and I' being sub-multiples of N and $\underline{i}$ and i' being the current relative indexes of the branches, in that the size in bytes of the first memory space is equal to $I \times (I - 1) \times M/2$ and the size in bytes of the second memory space is equal to $I' \times (I' - 1) \times M'/2$, and in that the sizes of the two memory spaces are parameterable by I, I', M and M'.

3. A device according to claim 2, characterized in that the memory (MM) is a random access memory, in particular a dual-port memory, the interleaving means and the deinterleaving means respectively include first addressing means (MDA1) and second addressing means (MDA2), said addressing means each include:

a first counter (CT1, CT10) defining the relative index i or i' of a branch,

a second counter (CT2, CT20) defining the number of bytes in a block and incremented each time that the first counter reaches its counting limit value,

a third counter (CT3, CT30) defining the current index of a block in the branch with index i or i' and incremented each time that a block contains M or M' bytes,

intermediate calculation means (MCI) calculating the address (adbs, adbs') of each branch in said memory from the content of the first counter,

the first addressing means (MDA1) further include first address determination means (MD1) adapted to determine successive read and write addresses in said memory of data successively delivered to the interleaving means and said first address determination means (MD1) determine said addresses from values supplied by the intermediate calculation means (MCI), the second and third counters (CT2, CT3) and the parameter M, and

the second addressing means (MDA2) further include second address determination means (MD2) adapted to determine successive read and write addresses in said memory of data successively delivered to the deinterleaving means and said second address determination means (MD2) determine said addresses from values supplied by the intermediate calculation means (MCI), the second and third counters (CT20, CT30), the parameter M' and the size (OF) of the first memory space.